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required for you to run this feature.. Much like Windows 10, Windows 10 Mobile uses a new version of the. of Windows 10 Mobile to a new version of the operating system,.1. Field of the Invention The present invention relates to a clock generator in a microcomputer, and more particularly, to a clock generator circuit for generating an accurate clock signal. 2. Description of the Related Art As a high performance microcomputer, one using a PLL (Phase Locked Loop) clock generator has been developed. A microcomputer of this type uses an IC having functions of a phase comparator for comparing the

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phases of a clock signal and a reference signal and a low-pass filter for filtering the output of the phase comparator with a threshold value to thereby output a voltage corresponding to a phase difference. By a voltage value output from the filter, a charge pump circuit is controlled, so that a DC output voltage is set to an IC input. The DC output voltage is supplied to a voltage-controlled oscillator (VCO) as a control voltage, thereby controlling the frequency of the clock signal. In a microcomputer of this type, by securing high accuracy of the PLL clock generator, the following advantages can be obtained: (1) A

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peripheral circuit of a microcomputer can be reduced in size. (2) A phase noise effect of the clock signal generated by the PLL clock generator can be reduced. The PLL clock generator is generally provided as an IC separate from a microcomputer, and connected to the microcomputer, for the following reason. (1) To reduce the size of the microcomputer. (2) To reduce the number of input/output pins of the microcomputer and the area of the package of the microcomputer. When the PLL clock generator is used for the above reasons, it is necessary to connect a plurality of ICs having

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the PLL clock generator in parallel in the microcomputer, or connect a plurality of PLL clock generators in parallel in the microcomputer to use a plurality of outputs of the respective PLL clock generators, thereby feeding a plurality of clock signals having different phases in the microcomputer. In order to reduce the area of the package of the microcomputer, the PLL clock generators are often disposed close to each other. In the

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